

[CONTROL CHIP AND METHOD FOR ACCELERATING MEMORY ACCESS]

Abstract of Disclosure

A control chip and operating method for accelerating memory access that can be applied to a memory system whose memory read command actual address is read from a system bus in a number of synchronous transmissions. On receiving a first section read address, the control chip operates to compare the first section read address with an identical bit portion of the write address of the memory-write commands inside a memory-write command queue. If the comparison indicates some difference, permission for executing the memory read command is granted. If the comparison indicates the presence of identical bits, a second section read address is received and compared with an identical bit portion of the write address of the memory-write commands inside a memory-write command queue. If the comparison indicates some difference, permission for executing the memory read command is granted. If the comparison indicates the presence of identical bits, permission for executing the memory read command is granted only after the memory-write command inside the memory-write command queue having an identical write address is executed.

Figures